Docket No.: 57454-257 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#7/C
And

In re Application of : **RESPONSE UNDER 37 CFR 1.116**
: **EXPEDITED PROCEDURE**

Fukashi MORISHITA :

Serial No.: 09/987,566 : Group Art Unit: 2816

Filed: November 15, 2001 : Examiner: Terry D. CUNNINGHAM

For: INTERNAL POWER SUPPLY VOLTAGE GENERATION CIRCUIT THAT CAN SUPPRESS REDUCTION IN INTERNAL POWER SUPPLY VOLTAGE IN NEIGHBORHOOD OF LOWER LIMIT REGION OF EXTERNAL POWER SUPPLY VOLTAGE

AMENDMENT UNDER 37 CFR 1.116

Box AF
Commissioner for Patents
Washington, DC 20231

Sir:

In response to the final Office Action dated July 17, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Enter for purposes of Appeal only. TDC 10/16/02

Claim 19 now reads as follows:

19. (Twice Amended) Level detection circuitry for detecting a difference between a first voltage and a second voltage, comprising:

a differential stage including a first insulated gate transistor and a second insulated gate transistor,